REMARKS/ARGUMENTS

Prior to this amendment, claims 1-15, 20-34, 36 and 37 were pending. In this amendment, no claims are amended, canceled, or added. Thus, claims 1-15, 20-34, 36 and 37 remain pending.

Interview

Applicants would like to thank the Examiner for extending the courtesy of a telephone interview with counsel, David B. Raczkowski, on May 1, 2009. Counsel provided a detailed explanation of the method embodied in claim 1 and the distinguishing characteristics relative to the cited references. Specifically, Counsel pointed out examples of the fixed-configuration secondary hardware, and how this hardware was used to implement some portions of a user design while the reconfigurable logic hardware may be used to implement other portions.

Claim Rejections – 35 USC § 112, Second Paragraph

Claims 1-15 and 20-34 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite regarding how ranking is made of the sets of input assignments when only one set of input assignments ("determining one or more sets of input assignments") is determined.

As described in the interview, the determining of a set of input assignments is performed for each of a plurality of portions of the user design. Specifically, claim 1 recites that "*determining ... one or more sets of input assignments*" is performed "*for each of a plurality of portions of the user design.*" Thus, there are a plurality of sets of input assignments, which may be ranked. Accordingly, Applicants respectfully request withdrawal of these rejections.

Claim Rejections – 35 USC § 103(a), Leaver, Young, Wallace

Claims 1-9, 20-28, and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leaver et al. (U.S. Patent No. 6,195,788 HI) in view of Young et al. (U.S. Patent No. 6,526,557).

Claim 1

Claim 1 is allowable over the cited references, either alone or in combination, as those references fail to teach or suggest all the elements of claim 1.

A. Leaver does not disclose fixed-configuration secondary hardware

For example, claim 1 recites determining an

> *implementation of a user design on a programmable device including a plurality of programmable logic elements, each comprising reconfigurable logic hardware and fixed-configuration secondary hardware, wherein the fixed-configuration secondary hardware has a plurality of inputs, the inputs common to at least two of the programmable logic elements*
>
> *for each of a plurality of portions of the user design, determining, with at least one processor of the computer system, one or more sets of input assignments of signals in the user design to the fixed-configuration secondary hardware, each set providing an implementation of a logic function of that portion of the user design using the fixed-configuration secondary hardware.*

Leaver maps a user design onto a programmable device. *See Leaver*, abstract. As part of the mapping, Leaver has two types of programmable logic elements (LUT and PTERM) of the programmable circuit that are used to implement the user design. *Id.*, col. 1 line 60 to col. 2 line 6. Figure 1C shows a LUT logic element.

Leaver breaks down the user design into logic cones, which have anchors in between the logic cones. *Id.*, FIGS. 4A-4C. For each logic cone, it is determined whether implementing the logic cone in a LUT or a PTERM is most efficient. *Id.*, col. 10 lines 1-40.

Thus, Leaver implements a user design with reconfigurable logic hardware (i.e. LUT or PTERM), but never mentions implementing portions of the user design with fixed-configuration secondary hardware.

At page 3, the Office Action cites to col. 7 lines 44-51 of Leaver, which describes anchors in the user design. However, the anchors are not part of the programmable device. Accordingly, Leaver does not teach or suggest determining sets of input assignments "*each set providing an implementation of a logic function of that portion of the user design using the fixed-configuration secondary hardware*" of a programmable logic element, as recited in claim 1.

Also, the anchors, as shown in FIGS 4A-4C, only have one input, not "*a plurality of inputs*." Note that col. 9 lines 28-35 mentions a node at an input or an output, but still only one input is ever mentioned.

The cited teachings of Young fail to make up for the deficiencies in Leaver.

B. Leaver does not rank and select sets of input assignments to the anchors

As another example, claim 1 recites:

> *ranking, with the processor, the sets of input assignments by determining a number of times each set is assigned to the fixed-configuration secondary hardware;*
>
> *selecting, with the processor, a highest ranked set of input assignments, wherein the highest ranked set is assigned to the fixed-configuration secondary hardware at least two or more times.*

The Office Action points to the determination of logic cones (separated by anchors) of the user design as determining inputs to a fixed-configuration hardware of the programmable device. *Id.*, col. 9 lines 19-67. Note that the Office Action has asserted that the anchors between the logic cones are the fixed configuration hardware.

At page 3, the Office Action then asserts that determining the relative cost of implementing a particular logic cone in a PTERM or a LUT corresponds to ranking inputs to the anchors. However, this is incorrect as the anchors are between the logic cones and not part of them. Thus, a determination of whether to implement a logic cone with a PTERM or a LUT does not involve the inputs to the anchors that are between the logic cones.

Note that the cited teaching of Young is for performing a ranking in a particular way. Since Leaver does not involve ranking the inputs to the anchors in any way, Young does not make up for this deficiency. Accordingly, Leaver and Young, alone or in combination, do not teach or suggest "*ranking... the sets of input assignments... to the fixed-configuration secondary hardware*," as recited in claim 1.

C. Young does not rank based on a number of times an assignment is made

Furthermore, Young is directed to a compression algorithm for configuration data for an FPGA. *See Young*, col. 1 lines 37-42. Young is not related to mapping a user design to an FPGA.

Regarding the compression algorithm, Young describes ranking a frame of data based on how similar it is to a previous frame of data, and not based on a number of assignments. *Id.*, col. 8 lines 6-20 and col. 9 lines 19-29. Young does not describe ranking any type of input assignment to anything. Accordingly, the combination of Leaver and Young do not teach or suggest "*ranking, with the processor, the sets of input assignments by determining a number of times each set is assigned to the fixed-configuration secondary hardware,*" as recited in claim 1.

For at least these reasons, claim 1 and its dependent claims are allowable over the cited references.

Other claims

Claims 20 and 36 should be allowed for similar reasons as claim 1. The other claims depend on one of the above claims and should be allowed for at least the same reasons and for the additional limitations they recite.

Claim 36 is also allowable for additional reasons. For example, claim 36 recites "*each programmable logic element comprising a register, a lookup table, and a plurality of logic gates having a plurality of inputs.*" At page 5, the Office Action points to FIG. 1C of Leaver as teaching this claim element, but does not state which elements of FIG. 1C correspond to which elements in the claim. FIG. 1C shows only a LUT and a register in the logic element, but no plurality of logic gates.

Young fails to make up for this deficiency. Accordingly, Leaver and Young do not teach or suggest this claim element. For at least this additional reason, claim 36 is allowable over the cited references.

Claim Rejections under 35 USC § 103(a), Leaver, Young, Wallace

Claims 10-15 and 29-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leaver et al. in view of Young and in further view of Wallace (US Patent No. 7,020,855). These claims respectively depend upon allowable independent claims 1 and 20, and are thus allowable. Note that the cited teachings of Wallace fail to make up for the deficiencies in Leaver and Young.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,

/David B. Raczkowski/

David B. Raczkowski
Reg. No. 52,145

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, Eighth Floor
San Francisco, California 94111-3834
Tel: 415-576-0200
Fax: 415-576-0300
DBR:scz
61836188 v1